IN THE CLAIMS:

Please amend the claims as follows:

Claims 1-6 (Cancelled)

Claim 7 (Original): A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate;

patterning the first metal layer to form a gate line, a gate electrode, a gate pad, a first shorting bar, and a second shorting bar;

forming a gate insulation layer, a pure amorphous silicon layer, a doped amorphous silicon layer and a second metal layer to cover the patterned first metal layer;

patterning the second metal layer and the doped amorphous silicon layer to form first, second and third through-holes and first and second grooves to expose a portion of the pure amorphous silicon layer, the first and second grooves creating an isolated portions of the second metal layer;

forming a passivation layer to cover the patterned second metal layer;

forming a source electrode, a drain electrode, a data line, a data pad, an insulating segment, and first, second and third contact holes; and

forming a pixel electrode, a first connector and a second connector of a transparent conductive material.

Claim 8 (Original): The method of fabricating an array substrate according to Claim 7, wherein the the gate electrode extends from the gate line, the gate pad is arranged at a first end of the gate line, and the first shorting bar and the second shorting bar are spaced apart from each other and arranged parallel with the gate line.

Claim 9 (Original): The method of fabricating an array substrate according to Claim 7, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode.

Claim 10 (Original): The method of fabricating an array substrate according to Claim 7, wherein the data pad is arranged at a first end of the data line, and the insulating segment is formed over the first shorting bar.

Claim 11 (Original): The method of fabricating an array substrate according to Claim 7, wherein the first contact hole penetrates the data pad, the second contact hole exposes a portion of the first shorting bar, and the third contact hole exposes a portion of the second shorting bar.

Claim 12 (Original): The method of fabricating an array substrate according to Claim 7, wherein the pixel electrode is connected with the drain electrode and is located in a pixel region defined by the gate line and the data line.

Claim 13 (Original): The method of fabricating an array substrate according to Claim 7, wherein the first connector electrically connects an odd numbered data line to the first shorting bar, and the second connector electrically connects an even numbered data lines to the second shorting bar.

Claim 14 (Original): The method of fabricating an array substrate according to Claim 7, wherein the first connector and the second connector contact the data pad through the first contact hole.

Claim 15 (Original): The method of fabricating an array substrate according to Claim 14, wherein the first connector contacts the first shorting bar through the second contact hole.

Claim 16 (Original): The method of fabricating an array substrate according to Claim 14, wherein the second connector contacts the second shorting bar through the third contact hole.

Claim 17 (Original): The method of fabricating an array substrate according to Claim 7, wherein the insulating segment is formed at a crossover point of the first shorting bar and the second connector.

Claim 18 (Original): The method of fabricating an array substrate according to Claim 17, wherein the insulating segment is disposed between the first shorting bar and the second connector.

Claim 19 (Original): The method of fabricating an array substrate according to Claim 18, wherein the insulating segment includes patterned layers comprising the passivation layer, the second metal layer, the doped amorphous silicon layer and the pure amorphous silicon layer.

Claim 20 (Original): The method of fabricating an array substrate according to Claim 7, wherein the transparent conductive material includes at least one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

Claim 21 (Original): The method of fabricating an array substrate according to Claim 7, wherein the first hole is formed over the gate electrode.

Claim 22 (Original): The method of fabricating an array substrate according to Claim 7, wherein the second hole is formed over the first shorting bar.

Claim 23 (Original): The method of fabricating an array substrate according to Claim 7, wherein the third hole is formed over the second shorting bar.

Claim 24 (Original): The method of fabricating an array substrate according to Claim 7, wherein the isolated metal layer is formed over the first shorting bar.

Claim 25 (Original): The method of fabricating an array substrate according to Claim 24, wherein the first groove and the second groove are formed on opposite sides of the isolated metal layer.

Claim 26 (Original): The method of fabricating an array substrate according to Claim 24, wherein the first groove is formed in a portion of the second metal layer between the first shorting bar and the second shorting bar.

Claim 27 (Original): The method of fabricating an array substrate according to Claim 7, wherein the second metal layer includes at least molybdenum (Mo) material.

Claims 28-32 (Cancelled)